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(54) Title: **PROCESS FOR MANUFACTURING A MICROELECTRONIC DEVICE**

(57) Abstract: The present invention relates to a process for manufacturing a microelectronic device, comprising providing a substrate with a photoresist image, coating the photoresist image with a shrink material, insolubilizing a portion of the shrink material in contact with the photoresist image, removing a portion of the shrink material which is not insolubilized with a removal solution, further where the removal solution comprises an aqueous solution of a surfactant.

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DescriptionProcess for Manufacturing a Microelectronic Device5 Technical Field

The present invention relates to a process for making an image on a substrate and a composition for developing such an image.

Background Art

10 The densification of integrated circuits in semiconductor technology has been accompanied by a need to manufacture very fine interconnections within these integrated circuits. Ultra-fine patterns are typically created by forming patterns in a photoresist coating using photolithographic techniques. Generally, in these processes, a thin coating of a film of a photoresist composition is first applied to a substrate material, such as silicon wafers used for making integrated circuits. The coated substrate is then baked to evaporate any solvent in the photoresist composition and to fix the coating onto the substrate. The baked coated surface of the substrate is next subjected to an image-wise exposure to radiation. This radiation exposure causes a chemical transformation in the exposed areas of the coated surface. Visible light, ultraviolet (UV) light, electron beam and X-ray radiant energy are radiation types commonly used today in microlithographic processes. After this image-wise exposure, the coated substrate is treated with a developer solution to dissolve and remove either the radiation-exposed or the unexposed areas of the photoresist.

25 Miniaturization of integrated circuits requires the printing of narrower and narrower dimensions within the photoresist. Various technologies have been developed to shrink the photoresist dimensions, examples of such technologies are, multilevel coatings, antireflective coatings, phase-shift masks, photoresists which are sensitive at shorter and shorter wavelengths, etc.

One important process for printing smaller dimensions relies on the technique of forming a thin layer on top of the image of the photoresist, which widens the photoresist image but reduces the dimension of the space between adjacent photoresist patterns. This narrowed space can be used to etch and define the substrate or be used to deposit materials, such as metals. This bilevel technique allows much smaller dimensions to be defined as part of the manufacturing process for microelectronic devices, without the necessity of reformulating new photoresist chemistries. The top layer or shrink material may be an inorganic layer such as a dielectric material, or it may be organic such as a crosslinkable polymeric material.

Dielectric shrink materials are described in US 5,863,707, and comprise silicon oxide, silicon nitride, silicon oxynitride, spin on material or chemical vapor deposited material. Organic polymeric coatings are described in US 5,858,620, where such coatings undergo a crosslinking reaction in the presence of an acid, thereby adhering to the photoresist surface, but are removed where the top shrink coating has not been crosslinked. US 5,858,620 discloses a method of manufacturing a semiconductor device, where the substrate has a patterned photoresist which is coated with a top layer, the photoresist is then exposed to light and heated so that the photogenerated acid in the photoresist diffuses through the top layer and can then crosslink the top layer. The extent to which the acid diffuses through the top coat determines the thickness of the crosslinked layer. The portion of the top layer that is not crosslinked is removed using a solution that can dissolve the polymer. US 5,858,620 discloses the top coat removal solution as being water or an aqueous solution of tetramethylammonium hydroxide.

It is critical to the performance of a microelectronic device which has been manufactured using a top shrink material that the open spaces in the photoresist layer be extremely clean after the removal of the

uncrosslinked material. Any residues left on the device can lead to defects and reduction in device yield.

If pure water is used as a removal solution, it is found that there is a strong tendency to form scum and photoresist residues in the spaces  
5 between the photoresist resist features. Another approach has been to use mixtures of water and organic water-miscible solvents, e.g., isopropanol. In the present invention, it has been surprisingly found that aqueous solutions of surfactants, particularly, anionic surfactants, are more selective in the removal of the insoluble part of the top layer, with the  
10 result that the open spaces are smaller, and furthermore, cleaner than is possible with water or mixtures of water and tetramethylammonium hydroxide or water-miscible solvents. The narrower spaces allow denser circuitry with faster switching speed to be defined with the microelectronic device.

15 The present invention relates to a process of coating a shrink material on top of an imaged photoresist, selectively crosslinking a portion of this layer, and removing the uncrosslinked portion of the layer with a removal solution, thereby reducing the space between the photoresist features, further, where the solution for removal of the uncrosslinked  
20 shrink material comprises an aqueous solution of a surfactant, particularly an anionic surfactant. It has been unexpectedly found that the use of this novel removal solution leads to improved pattern definition, higher resolution and improved cleanliness of the space between the imaged photoresist pattern.

#### Summary of the Invention

25 The present invention relates to a process for manufacturing a microelectronic device, comprising providing a substrate with a photoresist image, coating the photoresist image with a shrink material, insolubilizing  
30 a portion of the shrink material in contact with the photoresist image, removing a portion of the shrink material which is not insolubilized with a

removal solution, further where the removal solution comprises an aqueous solution of a surfactant. Preferably the surfactant is a nonionic surfactant, and more preferably an anionic surfactant, and even more preferably an anionic surfactant with an aliphatic chain having greater than  
5 7 carbon atoms.

#### Description of the Invention

The present invention relates to a process for manufacturing a microelectronic device, comprising forming a layer of shrink material on  
10 top of an imaged photoresist, crosslinking a portion of the shrink material near the photoresist interface, and removing the soluble portion with the removing solution, where the removing solution comprises an aqueous solution of a surfactant, preferably a nonionic surfactant, and more preferably an anionic surfactant, and even more preferably an anionic  
15 surfactant with an aliphatic chain having greater than 7 carbon atoms.

An imaged pattern of photoresist is formed on a substrate according to processes well-known to those skilled in the art.

Photoresists can be any of the types used in the semiconductor industry. There are two types of photoresist compositions, negative-  
20 working and positive-working. When negative-working photoresist compositions are exposed image-wise to radiation, the areas of the resist composition exposed to the radiation become less soluble to a developer solution (e.g. a cross-linking reaction occurs) while the unexposed areas of the photoresist coating remain relatively soluble to such a solution.  
25 Thus, treatment of an exposed negative-working resist with a developer causes removal of the non-exposed areas of the photoresist coating and the creation of a negative image in the coating, thereby uncovering a desired portion of the underlying substrate surface on which the photoresist composition was deposited.

30 On the other hand, when positive-working photoresist compositions are exposed image-wise to radiation, those areas of the photoresist

composition exposed to the radiation become more soluble to the developer solution (e.g. a rearrangement reaction occurs) while those areas not exposed remain relatively insoluble to the developer solution. Thus, treatment of an exposed positive-working photoresist with the developer causes removal of the exposed areas of the coating and the creation of a positive image in the photoresist coating. Again, a desired portion of the underlying surface is uncovered.

Positive working photoresist compositions are currently favored over negative working photo resists because the former generally have better resolution capabilities and pattern transfer characteristics. Photoresist resolution is defined as the smallest feature which the resist composition can transfer from the photomask to the substrate with a high degree of image edge acuity after exposure and development. In many manufacturing applications today, resist resolution on the order of less than one micron are necessary. In addition, it is almost always desirable that the developed photoresist wall profiles be near vertical relative to the substrate. Such demarcations between developed and undeveloped areas of the resist coating translate into accurate pattern transfer of the mask image onto the substrate. This becomes even more critical as the push toward miniaturization reduces the critical dimensions on the devices.

Generally, a photoresist comprises a polymer and a photosensitive compound. Examples of photoresist systems, without limitation, are novolak/diazonaphthoquinone, polyhydroxystyrene/onium salts, capped polyhydroxystyrene/onium salts, cycloaliphatic polymers/onium salts, etc. These photoresists are well-known for use at wavelengths ranging from 436nm to 193nm. Any type of photoresist that is capable of forming an image may be used. A photoresist is coated on a substrate, and the photoresist coating is baked to remove substantially all of the coating solvent. The coating is then exposed with the appropriate wavelength of light, and developed with a suitable developer.

Once a photoresist pattern is defined on the substrate, a shrink material comprising a polymer capable of becoming insoluble in the vicinity of a developed photoresist pattern, e.g., by crosslinking in the presence of an acid, and a solvent, where the solvent dissolves the polymer but not the photoresist, is coated over the substrate with the photoresist pattern. Typical examples of suitable systems for a shrink material that can crosslink in the presence of an acid are disclosed in US 5,858,620, and are polyvinyl acetal, a mixture of polyvinylacetal and methoxy-methylol-urea, a mixture of polyvinylacetal and methoxy-methylol-melamine, a mixture of methoxy-methylol-melamine and polyallyl-amine. Other systems capable of acid induced crosslinking may be used. The surface of the patterned photoresist may contain sufficient acid to induce crosslinking in the shrink material or, if desired, the photoresist may be exposed to generate additional amounts of acid. Alternatively, the photoresist surface may be treated with an acid solution before the shrink material is coated over the photoresist image. The shrink material is then crosslinked, where the time and temperature of the heating step (diffusion bake) is controlled to give a desired thickness for the crosslinker shrink film. Heating temperatures of the diffusion bake can range from about 100°C to about 160°C, preferably 110°C to about 130°C. The thickness of the shrink material that is crosslinked is dependent on the diffusion length of the acid. Flood exposure of the photoresist may be used to generate the acid. If selective exposure is desired then the photoresist may be exposed through a mask, which allows only specific areas to have the crosslinked shrink material, for example, the sides of the photoresist. The exposure dose determines the concentration of acid generated in the photoresist, and thus is an additional controlling factor in determining the final thickness of the crosslinked shrink film. As the thickness of the crosslinked shrink film increases, the space between the photoresist features becomes smaller, which allows smaller circuit geometries to be defined on the substrate.

The residual portion of the shrink material that is not crosslinked is removed using a novel removal solution. The novel removal solution comprises an aqueous solution of a surfactant, which may further comprise an alkali and/or a water-miscible solvent. Examples of an alkali are tetramethyl ammonium hydroxide, tetraethyl ammonium hydroxide, choline or mixtures thereof. Water-miscible solvents are, for example, lower aliphatic alcohols such as ethanol or isopropanol; multifunctional alcohols such as ethylene glycol, propylene glycol, glycerol, or their monomethyl ethers, in particular propylene glycol monomethyl ether (PGME). Water-soluble nonionic surfactants and anionic surfactants were found to provide good lithographic results. Examples of nonionic surfactants are ethylene oxide/propylene oxide polymers, terminated by alkynyl, fluoroalkyl, or aromatic groups. Anionic surfactants also gave superior lithographic performance, and examples of such surfactants are, salts of longer-chain alkanoic acids, such as laurates, stearates, or heptanoates, salts of alkyl or aralkyl sulfonic acids, such as laurylsulfonic acid, or variously substituted salts of sulfonic acid amides, or the partially or completely fluorinated derivatives of the above classes of compounds. Ammonium, tetramethyl ammonium, tetraethyl ammonium, or other alkyl ammonium ions are useful counterions. The actual composition of the removal solution is dependent on factors such as, the shrink material, the desired lithographic performance, compatibility of materials, production specifications, etc. It was found that for a particular product, AZ<sup>®</sup>R200 Coating, the best results were obtained with a removal solution comprising salts with long alkyl chains, particularly those with alkyl chain length greater than 7 carbons. Aliphatic hydrocarbon chains with greater than 7 carbons were particularly useful, since these give better wall profiles, clean development and narrower-space dimensions. -----

The removal solution is applied on the surface of the substrate in a manner known in the art. Puddle development, immersion development, spray development or any mixtures of these techniques may be used to



remove chemical compositions from the substrate. The time and temperature of the removal process is varied to give the best lithographic properties. Desirable lithographic properties being, for example, (a) cleanliness of the substrate after removal of the uncrosslinked shrink  
5 material, that is, the substrate is free from insoluble deposits, stringers, bridges, etc, (b) vertical wall angles, and (c) smooth surfaces.

At current resolution targets it is desirable to obtain a space reduction between photoresist features of from about 70nm to about 100nm. The exact space width reduction requirement is highly dependent  
10 on the type of microelectronic devices being manufactured.

Once the desired narrow space is formed as defined by the process described above, the device may be further processed as required. Metals may be deposited in the space, the substrate may be etched, the photoresist may be planarized, etc.

15 The following specific examples will provide detailed illustrations of the methods of producing and utilizing compositions of the present invention. These examples are not intended, however, to limit or restrict the scope of the invention in any way and should not be construed as providing conditions, parameters or values which must be utilized  
20 exclusively in order to practice the present invention.

## EXAMPLES

### Example 1

5           AZ<sup>®</sup>DX<sup>™</sup> 3200, a commercial deep uv (DUV) photoresist, available from Clariant Corporation (Somerville, New Jersey), was spin-coated at 1360 rpm onto 6" wafers, baked at 85°C for 90 sec to give a film thickness of 760 nanometers(nm), followed by exposure on an ASML  
10 PAS5500/300B DUV stepper set at NA = 0.60 and sigma = 0.6, post exposure baked at 115 °C for 90 sec and developed in AZ<sup>®</sup> MIF300 Developer (2.38% w/w tetramethyl ammonium hydroxide, available from Clariant Corporation, Somerville, New Jersey). 190nm equal line and space structures were found upon inspection after development of the  
15 photoresist.

          The wafers were then coated with the shrink material, AZ<sup>®</sup> R200 Coating, a polyvinylalcohol/crosslinker coating (available from Clariant Corporation, Somerville, New Jersey) at a spin speed of 2500 rpm, baked at 85 °C for 70 sec, and baked(diffusion bake) again at 110 °C for 70 sec  
20 to crosslink the shrink material. The film thickness of the AZ<sup>®</sup> R200 layer was determined to be 750 nm on a separate bare silicon monitor wafer. Removal solutions 2-5 were prepared with a concentration of 1weight% of various surfactants in water as listed in Table 1. The wafers were developed with these removal solutions by manually puddling 20 ml of the  
25 removal solution on the wafer for 60 sec, followed by a deionized water rinse. Table 1 compares the effectiveness of removal solutions 1-5 in reducing space width, cleanliness of development, and sidewall angle.

### Example 2

30           A deep uv photoresist based on an acetal-protected poly(4-hydroxystyrene) was applied to silicon wafers, exposed to DUV light through a mask and processed to give isolated space features ranging in

space width from 280 to 180 nm. The wafers were then coated with AZ<sup>®</sup>R200 Coating as described in Example 1, with the exception that the diffusion bake process was as specified in column 2 of Table 2. The chemical compositions of the experimental removal solutions are given in Table 3. The results of the processes are given in Table 2.

The target of this experiment was to find a removal solution that made it possible to achieve a reduction in the printed space width from about 200 nm to about 100 nm. The results of the experiment are given in Table 2. It was found that with commercial AZ<sup>®</sup>R2 Developer, it was not possible to achieve a shrink to 100 nm space width even if a higher diffusion bake of 120°C for 70 sec was applied. Similarly, water did not provide the needed lithographic performance.

Only removal solutions with surfactants and with optimized processing conditions provided the required lithographic performance. Removal solution with an anionic surfactant made it possible to consistently print isolated spaces close to the target. The investigation of the performance as a function of the diffusion bake (experiments 11-13) shows that the process also has good temperature latitude.

### Example 3:

A deep uv photoresist based on a copolymer of 4-hydroxystyrene and t-butyl acrylate was applied to silicon wafers, exposed to DUV light through a mask and processed to give isolated space features ranging from 280 to 180 nm. The wafers were then coated with AZ<sup>®</sup>R200 Coating as described in Example 1, with the exceptions that the bake process was as specified in column of Table 4, and the composition of the removal solution is specified in the third column of Table 4. The compositions of the removal solutions are given in Table 3. Results of the experiment are given in the remaining columns of Table 4, where the experimental solutions are compared with the commercial AZ<sup>®</sup>R2 Developer.

The target of the experiment was to find removal solutions and processing conditions that make it possible to achieve a reduction in space width from 200nm to about 100 nm. The results of the experiment are given in Table 3. It was found that when using AZ®R200 Coating with  
 5 AZ®R2 Developer, although some space shrinkage is obtained, however, it was not possible to achieve a target space shrinkage of 100 nm space width even if a higher diffusion bake of 120°C for 70 sec was applied. Removal solutions, A1 and A2, which are based on an anionic surfactant, show no bridging and give clean development for isolated spaces close to  
 10 the target. As the concentration of the surfactant was varied the space width that could be achieved also changed. The optimum surfactant concentration varies with the chemical composition of the photoresist and the shrink material.

15

Table 1: Comparison of results for different removal solutions for Example 1.

Removal Solutions	Surfactant	Initial Space[nm]	Final Space [nm]	Cleanliness	Sidewall
1	AZ®R2 Developer	310	212	bridging	sloped
2	TMA stearate	310	219	clean	vertical
3	TMA laurate	310	227	clean	vertical
4	ALS	310	195	clean	vertical
5	TMA heptanoate	310	178	bridging	vertical

20 AZ®R2 Developer: 5 wt% isopropanol in water  
 TMA: tetramethyl ammonium,  
 ALS: ammonium lauryl sulfate

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Table 2: Comparison of results for different removal solutions for Example 2.

Experiment #	Diffusion Bake	Developer	Image Quality	Initial Space CD [nm]	Shrunk Space CD [nm]
1	120°C/70sec	AZ®R2	Bridging	200	120
2	120°C/70sec	C3		220	190
3	120°C/70sec	water		---	---
4	120°C/70sec	C1	Scum	200	100
5	120°C/70sec	B3	Bridging	280	180
7	120°C/70sec	D3		200	100
8	120°C/70sec	D2	Bridging	200	100
9	120°C/70sec	D3	Bridging	280	180
11	110°C/70sec	A3		180	121
12	115°C/70sec	A3		180	104
13	120°C/70sec	A3		190	104

5

Table 3: Composition of the removal solutions

Name	Removal Solution Composition
A1	1,000 ppm of Sol. 1 in water
A2	50 ppm of Sol. 1 in water
A3	20,000 ppm of Sol. 1 in water
B1	50 ppm w/w Macol 16 surfactant in water
B2	1,000 ppm w/w Macol 16 surfactant in water
B3	10,012 ppm w/w Macol 16 surfactant in water
C1	50 ppm w/w Surfynol 440 surfactant in water
C2	1,000 ppm w/w Surfynol 440 surfactant in water
C3	10,000 ppm w/w Surfynol 440 surfactant in water
D1	B1 : Sol. 2 = 1:1
D2	5% isopropanol in B3
D3	10% isopropanol in B3
Sol. 1	3.5% w/w ALS in 2.38% w/w TMAH in water

Macol 16 is available from PPG Industries.

10 Surfynol 440 is available from Air Products Corp.

Table 4: Comparison of results for different removal solutions for Example 3.

Wafer #	Diffusion Bake	Removal solution	Initial CD nm	Shrunk CD nm
1	110°C/70sec	AZ®R2	180	160
2	110°C/70sec	C3	---	---
3	120°C/70sec	AZ®R2	200	180
4	120°C/70sec	AZ®R2	200	140
5	120°C/70sec	D1	200	150
6	120°C/70sec	A1	190	111
7	120°C/70sec	A2	190	102
8	123°C/70sec	A3	200	144
9	123°C/70sec	A1	190	109
10	126°C/70 sec	A1	190	108
11	126°C/70 sec	A3	200	152
12	120°C/70sec	A1	180	99

- 8) The process according to claim 1, further comprising treating the photoresist with an acid solution prior to coating the photoresist with the shrink material.
- 5 9) The process according to claim 1, further comprising heating the shrink material after step b), and thereby insolubilizing a portion of the shrink material.
- 10 10) The process according to claim 9, where the heating temperature ranges from 100°C to 160°C.
- 11) The process according to claim 1, further where the surfactant is a non-ionic surfactant.
- 15 12) The process according to claim 1, further where the surfactant is an anionic surfactant.
- 13) The process according to claim 12, further where the anionic surfactant has an alkyl chain greater than 7 carbon atoms.
- 20 14) A removal solution comprising an aqueous solution of a surfactant.
- 15) The removal solution of claim 14, where the surfactant is a non-ionic surfactant.
- 25 16) The removal solution of claim 14, where the surfactant is an anionic surfactant.
- 17) The removal solution of claim 16, where the anionic surfactant has an alkyl chain greater than 7 carbon atoms.
- 30

## CLAIMS

- 1) A process for manufacturing a microelectronic device, comprising;
- 5 a) providing a substrate with a photoresist image;
- b) coating the photoresist image with a shrink material;
- c) insolubilizing a portion of the shrink material in contact with the photoresist image;
- 10 d) removing a portion of the shrink material which is not insolubilized with a removal solution, further where the removal solution comprises an aqueous solution of a surfactant.
- 2) The process according to claim 1, where the removal solution further comprises an a hydroxide base.
- 15 3) The process according to claim 1, where the removal solution further comprises a water-miscible solvent.
- 4) The process according to claim 2, where the removal solution further comprises a water-miscible solvent.
- 20 5) The process according to claim 1, further comprising exposing the shrink material after coating the photoresist image.
- 6) The process according to claim 5, further comprising imagewise exposing the shrink material.
- 25 7) The process according to claim 5, further comprising flood exposing the shrink material.
- 30



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- (74) Agent: **HÜTTER, Klaus**; Clariant Service GmbH, Patente, Marken, Lizenzen, Am Unisys-Park 1, 65843 Sulzbach (DE).
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## B. FIELDS SEARCHED

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)  
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## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
E	US 6 319 853 B1 (TOYOSHIMA TOSHIYUKI ET AL) 20 November 2001 (2001-11-20) column 2, line 53 - line 54; claim 3	1,3
X	& DE 198 43 179 A (MITSUBISHI DENKI KK ) 22 July 1999 (1999-07-22)	1,3
X	EP 0 920 852 A (TAKASAGO PERFUMERY CO LTD) 9 June 1999 (1999-06-09) paragraph '0041!; examples	14-17
Y	US 5 858 620 A (TOYOSHIMA TOSHIYUKI ET AL) 12 January 1999 (1999-01-12) cited in the application the whole document	1-3
	-/-	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Name and mailing address of the ISA

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, Y	US 2001/003481 A1 (SUGAWARA HIROSHI) 14 June 2001 (2001-06-14) paragraphs '0004!', '0005!	1-3
Y	& JP 2000 138150 A (ORGANO CORP ) 16 May 2000 (2000-05-16)	1-3
A	DE 198 14 142 A (MITSUBISHI ELECTRIC CORP) 15 October 1998 (1998-10-15) claim 10; examples	1
A	DE 199 15 899 A (RYODEN SEMICONDUCTOR SYST ENG ;MITSUBISHI ELECTRIC CORP (JP)) 17 February 2000 (2000-02-17) column 4, line 8 - line 16; claim 1	1
P, A	WO 01 25854 A (CLARIANT INT LTD ;KANDA TAKASHI (JP); TANAKA HATSUYUKI (JP)) 12 April 2001 (2001-04-12) abstract	1
P, A	DE 100 14 083 A (RYODEN SEMICONDUCTOR SYST ENG ;MITSUBISHI ELECTRIC CORP (JP)) 22 March 2001 (2001-03-22) column 5, line 33 - line 45; example 1	1

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Information on patent family members

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6319853	B1	20-11-2001	JP 3189773 B2 JP 11204399 A DE 19843179 A1 IT MI982032 A1 TW 393699 B	16-07-2001 30-07-1999 22-07-1999 20-03-2000 11-06-2000
EP 0920852	A	09-06-1999	EP 0920852 A2 JP 11222416 A US 6379659 B1	09-06-1999 17-08-1999 30-04-2002
US 5858620	A	12-01-1999	DE 19706495 A1 JP 3071401 B2 JP 10073927 A KR 218217 B1	08-01-1998 31-07-2000 17-03-1998 01-09-1999
US 2001003481	A1	14-06-2001	JP 2000138150 A US 6187519 B1	16-05-2000 13-02-2001
DE 19814142	A	15-10-1998	JP 3071401 B2 JP 10073927 A CN 1199922 A DE 19814142 A1 IT MI980673 A1	31-07-2000 17-03-1998 25-11-1998 15-10-1998 30-09-1998
DE 19915899	A	17-02-2000	JP 2000058506 A CN 1244723 A DE 19915899 A1 TW 414963 B	25-02-2000 16-02-2000 17-02-2000 11-12-2000
WO 0125854	A	12-04-2001	JP 2001109165 A WO 0125854 A1	20-04-2001 12-04-2001
DE 10014083	A	22-03-2001	JP 2001066782 A DE 10014083 A1	16-03-2001 22-03-2001